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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,471	05/03/2001	Sukeyuki Shinotsuka	263/196	6954
22249	7590	02/09/2005	EXAMINER	
LYON & LYON LLP 633 WEST FIFTH STREET SUITE 4700 LOS ANGELES, CA 90071			YAM, STEPHEN K	
			ART UNIT	PAPER NUMBER
			2878	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/848,471

Applicant(s)

SHINOTSUKA ET AL.

Examiner

Stephen Yam

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 May 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 0501.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the image sensor of Claim 1 (which Fig. 1 cannot illustrate since it is labeled as "Prior Art", thereby denoting Applicant's admitted prior art) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The disclosure is objected to because of the following informalities:

Paragraph 0002 refers to Fig. 1 as illustrating a typical conventional image sensor, but Paragraph 0011 refers to Fig. 1 as an embodiment of the present invention. It is unclear what portion of Applicant's disclosure is admitted prior art and which portion is Applicant's claimed inventive novelty.

Appropriate correction is required.

***Claim Objections***

4. Claims 3 and 4 are objected to because of the following informalities:

In Claim 3, line 4, "logarithmic characteristic" should be replaced with "logarithmic output characteristic" for clarity.

In Claim 4, it is unclear whether any of the first, second, or third transistors are related to the MOS type transistor defined in parent Claims 1-3, as no relationship is defined.

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

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5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonemoto US Patent No. 5,808,677.

Regarding Claims 1-3, Yonemoto teaches (see Fig. 3, 7, and 9) an image sensor comprising a number of light sensor circuits (1), each of which represents a unit pixel (see Fig. 3) and is capable of producing in a photoelectric converting element (1) a sensor current proportional to the quantity of light falling thereon (see Col. 5, lines 19-22) and converting the current into a voltage signal (see Col. 5, lines 19-30 and 46-47) by a MOS type transistor (1) with a logarithmic output characteristic in a weak inverse state (see Col. 12, lines 14-22- since the transistor is operating in the weak inversion region, it is providing a logarithmic output), and a means (15, 31) for removing a charge accumulated in a parasitic capacity of the photoelectric converting element (see Col. 7, lines 4-16) by changing a source voltage of the transistor (source connected to vertical signal line- see Col. 7, lines 27-33) to a value ( $V_{RB}$ ) lower than a normal value (see Col. 8, lines 50-57) to initialize each pixel before detecting a light signal (see Col. 7, lines 41-51). Regarding Claim 2, Yonemoto et al. also teach the light sensor circuits arranged to form a matrix of pixels (see Col. 4, lines 35-38), and the means for removing a charge as a voltage switching-over circuit (see Col. 7, lines 27-38). Regarding Claim 3, Yonemoto also teach (see Fig. 3) a pixel-line selecting circuit (8) for successively selecting pixel lines ( $n$ ,  $n+1$ , ...) (see Col. 1, lines 46-51), and a pixel selecting circuit (2) for successively selecting pixels ( $m$ ,

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m+1, ...) in one selected line (see Col. 5, lines 46-57), both of said selecting circuits cooperating together to successively scan and read sensor signals from respective pixels in a time series (see Col. 4, line 64-Col. 5, line 4 and Col. 5, lines 46-57). Yonemoto does not teach changing the drain voltage of the transistor. It is well known in the art to select between NMOS and PMOS conductivity-type transistors, and that the source node for one conductivity-type transistor becomes the drain node for the other conductivity-type transistor. It would have been obvious to one of ordinary skill in the art at the time the invention was made to change the drain voltage instead of the source voltage of the transistor by using the alternative conductivity-type transistor, in the sensor of Yonemoto, to provide easier fabrication and integration with other transistor devices on a substrate, as appropriate.

7. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonemoto in view of Hoffman US Patent No. 6,252,462.

Regarding Claim 4, Yonemoto teaches the sensor in Claims 1-3, according to the appropriate paragraph above. Yonemoto also teaches the light sensor circuit having a first transistor (1) for converting a sensor current flowing in the photoelectric converting element to a voltage signal (see Col. 5, lines 19-30 and 46-47) by using its logarithmic output characteristic in a weak inverse state (see Col. 12, lines 14-22- since the transistor is operating in the weak inversion region, it is providing a logarithmic output). Yonemoto does not teach a second transistor for amplifying the voltage signal and a third transistor for outputting a sensor signal corresponding to the amplified voltage signal at a specified moment of time. Hoffman teaches (see Fig. 2) a similar device, with a light sensor circuit (10) with a second transistor (12) for

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amplifying a voltage signal and a third transistor (20) for outputting a sensor signal corresponding to the amplified voltage signal at a specified moment of time (see Col. 4, lines 64-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a second transistor for amplifying the voltage signal and a third transistor for outputting a sensor signal corresponding to the amplified voltage signal at a specified moment of time in the light sensor circuit, as taught by Hoffman, in the sensor of Yonemoto, to provide greater signal strength for improved detection contrast, and provide improved signal isolation on the pixel output line.

Regarding Claim 5, Yonemoto teaches the sensor in Claim 3, according to the appropriate paragraph above. Yonemoto does not teach a sample-and-hold circuit provided on an output side of each pixel in each pixel line. Hoffman teaches (see Fig. 2) a similar device, with a sample-and-hold circuit provided on an output side of each pixel in each pixel line (see Col. 1, lines 44-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a sample-and-hold circuit provided on an output side of each pixel in each pixel line, as taught by Hoffman, in the sensor of Yonemoto, to provide enhanced signal capture and handling such as correlated-double-sampling and analog-digital conversion.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (571)272-2449. The examiner can normally be reached on Monday-Friday 8:30am-5pm.


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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (571)272-2444. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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THANH X. LUU  
PATENT EXAMINER